

## Claims

- [c1] What is claimed is:
- 1.A method for determining an operating voltage of floating point error detection of a central processing unit (CPU) through a control circuit; said CPU comprising a first output port, wherein said first output port is floating when said operating voltage of floating point error detection of said CPU is higher than a first predetermined voltage level, and said first output port is connected to a grounding when said operating voltage of floating point error detection of said CPU is lower than said first predetermined voltage level; said control circuit comprising a test port connected to the first output port of said CPU for determining said operating voltage of floating point error detection of said CPU; said method comprising:
- providing a power supply connected to the first output port of said CPU via a resistor for supplying a first voltage level; and
- measuring a voltage level at said test port of said control circuit to determine said operating voltage of floating point error detection of said CPU.
- [c2] 2.The method of claim 1 wherein said first voltage level is a positive voltage, said operating voltage of said CPU is higher than said first predetermined voltage level when said voltage level at said test port of said control circuit is higher than a second predetermined voltage level, and said operating voltage of said CPU is lower than said first predetermined voltage level when said voltage level at said test port of said control circuit is lower than said second predetermined voltage level.
- [c3] 3.The method of claim 1 wherein said control circuit is a south bridge chipset.
- [c4] 4.The method of claim 1 wherein said CPU further comprises a second output port connected to a signal input port of said control circuit for transmitting a predetermined signal;
- said method further comprising:
- determining information contained in said predetermined signal according to said operating voltage of floating point error detection of said CPU.
- [c5] 5.The method of claim 4 wherein said predetermined signal is a floating point

Year	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1970	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100